



# VMM Adopter Class

## 2 days



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The Verification Methodology Manual for SystemVerilog (VMM) specifies a functional verification methodology, and defines the VMM Standard Library implemented in SystemVerilog. VMM includes constrained random stimulus generation, functional coverage collection, assertions, and transaction-level modelling. VMM's layered structure and channel-based communication model make it suitable for building both very simple and very complex functional verification environments

Delegates for this course must start with a working knowledge of SystemVerilog, including its object-oriented programming (class-based) features. This course takes delegates through to full VMM verification project readiness by focussing on the verification principles and the in-depth practical application of the VMM using Synopsys VCS™.

Workshops comprise approximately 50% of class time, and are based around carefully designed exercises to reinforce and challenge the extent of learning. In the hands-on workshops, delegates will progressively build a complete VMM verification environment for a small example system.

### Who should attend?

- Verification engineers who need to develop, deploy or configure SystemVerilog verification environments based on the VMM
- Design engineers who wish to make use of SystemVerilog's verification capabilities for test bench development using the VMM using the AVM

### What will you learn?

- The principles of effective functional verification using SystemVerilog
- How to understand the VMM Standard Library classes, documentation and examples
- How to build complete, powerful, reusable VMM-compliant verification environments

### Pre-requisites

A sound working knowledge of SystemVerilog, including some experience with its object-oriented programming features, is essential. For engineers new to SystemVerilog the Doulos [Comprehensive SystemVerilog](#) course, or equivalent, is an essential prerequisite.

For team-based courses, precursor training in SystemVerilog can be tailored to the team's specific profile using our [Modular SystemVerilog](#) portfolio. Contact Doulos to discuss options that suit your needs.

### Training materials

Doulos training materials are renowned for being the most comprehensive and user friendly available. Their style, content and coverage is unique in the EDA training world, and has made them sought after resources in their own right. Fees include

- Fully indexed class notes creating a complete reference manual
- Lab files comprising the complete SystemVerilog source files and scripts

# Structure and Content

## Introduction

Course structure • motivation • principles • benefits • overview of VMM testbench architecture

## Verification Methodology

Assertion based verification • functional coverage • structural coverage • constrained random • coverage-driven verification • the verification process • verification planning • coverage models

## Class OOP-Refresher (if required)

Object-Oriented Programming • class • object • method • constructor • static members • inheritance • overriding • virtual method • up-casting • down-casting using \$cast

## Modelling Transaction Data

The VMM-compliant transaction data model • implementing a VMM data factory • copy and compare methods • using the vmmgen script

## Connecting a testbench to the DUT

Connecting classes to the DUT: signal drive from a program • clocking, interfaces and modports working together • VMM-compliant connection to the DUT using virtual interfaces • active and passive command-level transactors

## Building a simple Verification environment

Transaction data at higher levels of the testbench: VMM channels • Creating transaction stimulus: the VMM atomic generator • Putting it all together: constructing a complete VMM environment • The environment's execution phases • Controlling testbench execution

## Customising an environment

Introducing directed tests • VMM callbacks for checking and error injection • Callback façade classes

## Constrained Randomization

Constrained random stimulus • tlm\_fifo • standard blocking and non-blocking interfaces • put / get / peek • constraints in SystemVerilog • controlling the constraint solver • Lab - constrained random stimulus

## Monitoring and Checking

Monitoring and self-checking: using callbacks to connect a scoreboard • Coverage sampling and transaction coverage

## Communication and Synchronisation

The notification service • ONE\_SHOT, ON\_OFF and BLAST notifications • Creating your own notifications • Conventional standard notifications in transactions and transactors • The message logging service • Message severity, verbosity and customisation • Building a logger hierarchy

## Advanced Stimulus Generation

The scenario generator • writing your own scenarios • adding custom scenarios to the testbench • hints for creating robust scenario constraints • debugging and keeping track of scenarios

## Further Opportunities

Overview of other aspects of VMM: assertions, XVCs • verification IP under VMM • integrating legacy code • the register abstraction layer (RAL) and hierarchical environment composition